Experiment No. 06

Aim: To study different types of flip-flops and Verification of Truth table of FFs. ALSO, to study, design and implement various asynchronous counters and its timing diagram analysis.

# Objectives:

1. To study various FFs and understand merits and demerits of FFs.
2. To understand specification parameters of FFs.
3. To understand excitation table of FFs.
4. To study various counters.
5. To understand and realization of asynchronous counters.
6. To analyze timing diagram of counters.
7. To understand real life applications of FFs and Counters.

# Equipment:

ICs, regulated power supply, bread board, connecting wires, DMM, etc.

# Theory:

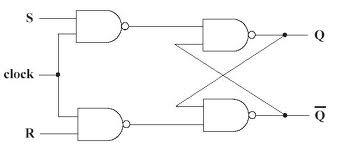
## Introduction to Flip-flops:

In electronics, a flip-flop or latch is a circuit that has two stable states and can be used to store state information.  It is the basic storage element is sequential logic. Flip-flops can be either simple or clocked; the simple ones are commonly called latches. The word *latch* is mainly used for storage elements, while clocked devices are described as *flip-flops*.

Flip-flops can be divided into common types: the **SR** ("set-reset"), **D** ("data" or "delay"[]](http://en.wikipedia.org/wiki/Flip-flop_(electronics)#cite_note-16)), **T** ("toggle"), and **JK** types are the common ones.

## SR Flip-flop:

The circuit diagram of SR flip-flop using NAND gates and using a clock pulse is as shown below-



Truth table for SR FF:

|  |  |  |
| --- | --- | --- |
| Inputs | Outputs |  |
| J K Clk | Q Q’ | Comments |
| 0 0 H | Q Q’ | No change |
| 0 1 H | 0 1 | RESET |
| 1 0 H | 1 0 | SET |
| 1 1 H | Q’ Q | Toggle |

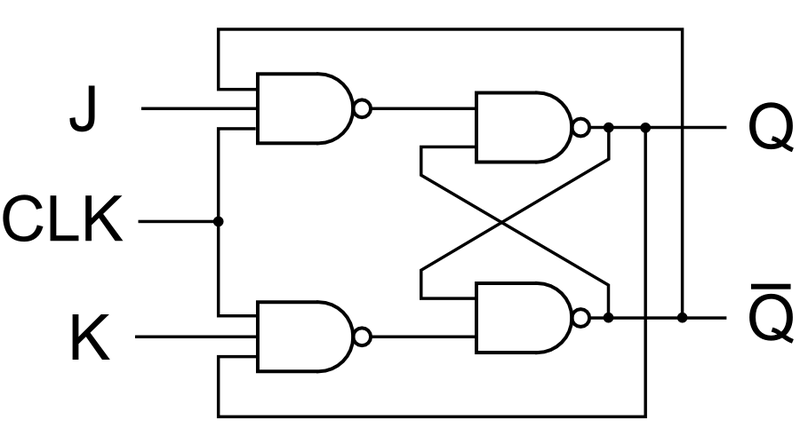
Operation on SR FF

1. S=R=0,no change
2. S=0, R=1, Q (t+1) =0. This is the reset condition.
3. S=1, R=0, Q (t+1) =1.This is set condition.
4. S=R=1, this is forbidden condition.

The last state in SR flip-flop i.e. S=R=1 is prohibited, so to overcome this JK flip flop is designed.

## JK Flip-flop:

The circuit diagram of JK flip-flop is as shown below-



Its truth table is-

|  |  |
| --- | --- |
| J K | Q(t+1) |
| 0 0 | Q(t) (no change) |
| 0 1 | 0 (reset) |
| 1 0 | 1 (set) |
| 1 1 | Q’ (t) |

Operation:-

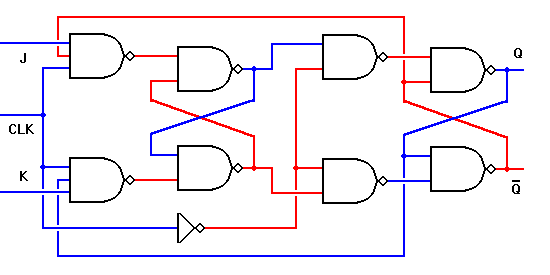
The operation of JK flip flop is as shown in the truth table.

Here when both inputs are zero i.e. J=K=1, After a time interval equal to propagation delay of two NAND gates in series, the o/p will change Q=1 and after another time interval, the o/p will change to Q=0.Hence,the o/p will oscillate between Q=1 and Q=0. At the end of clock pulse, the value of Q is uncertain. This situation is referred as race around condition.

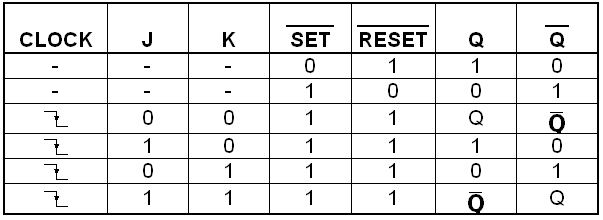
JK flip flop has a restriction of race around condition which is overcome by Master slave flip-flop.

## Master-slave flip flop-

The circuit diagram is



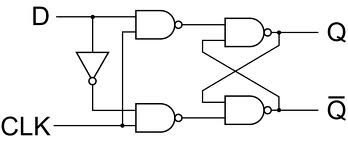
Its truth table is

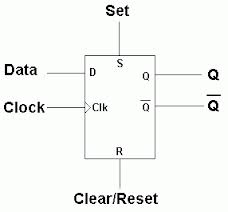


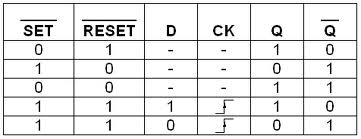
Operation:-

The working of master slave JK flip flop is as shown in the truth table.

## D-flip flop:





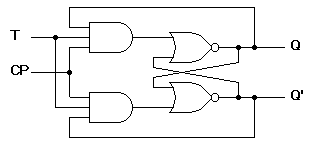


Operation:

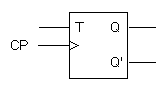
If we use only middle two rows of the truth table of SR or JK flip flop, we obtain D type flip flop. It has only one i/p i.e. D i/p or data i/p. Q (t+1) is equal to D.

## T-flip flop-

The circuit diagram is-



Logic symbol is:



Its truth table is-

Operation:-

In JK flip-flop, if J=K, the resulting flip-flop is T type Flip-flop. It has only one input, referred as T input. The truth table as shown.

## Introduction to COUNTERS: -

Counters

     Counter is the most useful and versatile subsystem of digital branch. Counter is going to count number of clock pulses applied to it. Maximum count that binary counter can count is 2n- 1. Clock pulses occur at regular time interval, so that counter can be used to measure time or frequency. Digital counters are integrated circuits (ICs) that count events in computers and other digital systems. Because they must remember past states, digital counters include memory. Generally, digital counters consist of bistable devices or bistable multi vibrators called flip-flops. The number of flip-flops and the way in which they are connected determines the number of states and the sequence of states that digital counters complete in each full cycle.

Counters can be subdivided into 2 groups:

* Asynchronous Counters
* Synchronous Counters

The way in which devices are clocked determines whether digital counters are categorized as synchronous or asynchronous. In synchronous devices (such as synchronous BCD counters and synchronous decade counters), one clock triggers all of the flip-flops simultaneously. With asynchronous devices, often called asynchronous ripple counters an external clock pulse triggers only the first first-flop. Each successive flip-flop is then clocked by one of the outputs (Q or Q') of the previous flip-flop. Digital counters are configured as [UP](http://www.globalspec.com/datasheets/3539/areaspec/counter_direction_up) (counting in increasing sequence), DOWN (counting in decreasing sequence) or Bidirectional (UP / DOWN).

Synchronous / Asynchronous counter can be subdivided into following subgroups:

* Sequential counters: States of counter are sequential.
* Non-sequential Counters: Sequence or states of counter are sequential but irregular.
* Regular Counters: In this counters, FFs are used. There is direct relation between number of states and number of FFs used i.e. N=2m.
* Decade counter – counts through ten states per stage.
* Up down counter – counts both up and down, under command of a control input.
* Ring counter – formed by a shift register with feedback connection in a ring.
* Johnson counter – a twisted ring counter.
* Cascaded counter.

  Some of the commercial ICs used for design of Counters:

* IC 7490-Decade Counter
* IC 7492 Divide by 10 Counter
* IC 7493 4 - bit binary Counter
* IC 74190 Up -Down Decade Counter

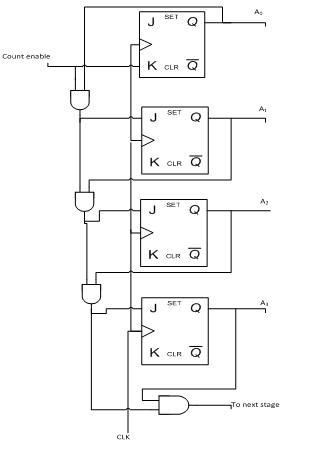
## Synchronous Decade Counters:

        Similar to an asynchronous decade counter, a synchronous decade counter counts from 0 to 9 and then recycles to 0 again.  This is done by forcing the 1010 state back to the 0000 state.  This so called truncated sequence can be constructed by the following circuit.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| |  |  |  |  |  | | --- | --- | --- | --- | --- | | **Clock Pulse** | **Q3** | **Q2** | **Q1** | **Q0** | | 0 | 0 | 0 | 0 | 0 | | 1 | 0 | 0 | 0 | 1 | | 2 | 0 | 0 | 1 | 0 | | 3 | 0 | 0 | 1 | 1 | | 4 | 0 | 1 | 0 | 0 | | 5 | 0 | 1 | 0 | 1 | | 6 | 0 | 1 | 1 | 0 | | 7 | 0 | 1 | 1 | 1 | | 8 | 1 | 0 | 0 | 0 | | 9 | 1 | 0 | 0 | 1 |   ***Table:****Sequence for Synchronous Decade Counter* |

* Q0 toggles on each clock pulse.
  + Q1changes on the next clock pulse each time Q0=1 and Q3=0.
  + Q2 changes on the next clock pulse each time Q0= Q1=1.
  + Q3 changes on the next clock pulse each time Q0=1, Q1=1 and Q3=1 (count 7), or when Q0 =1 and Q3=1 (count 9).

         Asynchronous counter circuit design is based on the fact that each bit toggle happens at the same time that the preceding bit toggles from a "high" to a "low" (from 1 to 0).  Since we cannot clock the toggling of a bit based on the toggling of a previous bit in a synchronous counter circuit (to do so would create a ripple effect) we must find some other pattern in the counting sequence that can be used to trigger a bit toggle.

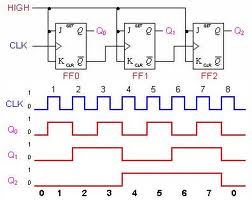


*4-bit Synchronous Binary Counter*

## Asynchronous decade counter:

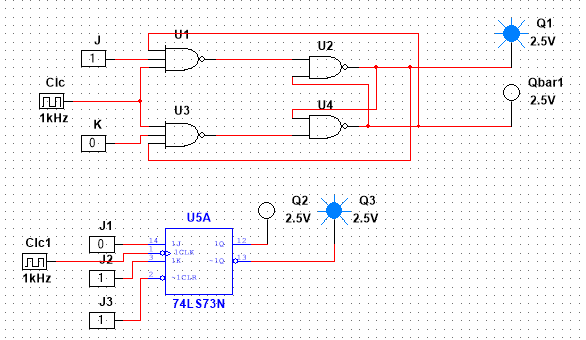
A common modulus for counters with truncated sequences is ten. A counter with ten states in its sequence is called a decade counter.  The circuit below is an implementation of a decade counter. Once the counter counts to ten (1010), all the flip-flops are being cleared.  Notice that only Q1 and Q3 are used to decode the count of ten.  This is called partial decoding, as none of the other states (zero to nine) have both Q1 and Q3 HIGH at the same time.

3-bit UP counter is as shown below:

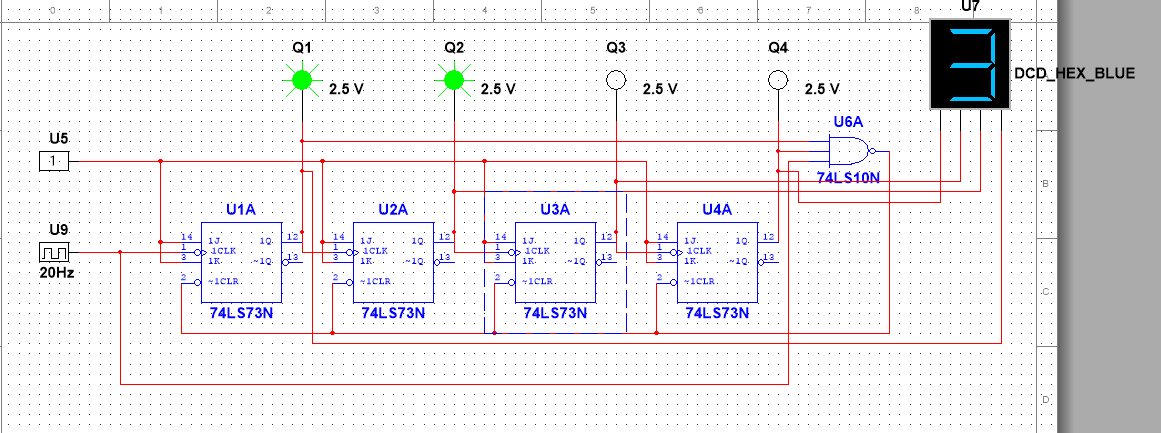


# Design:

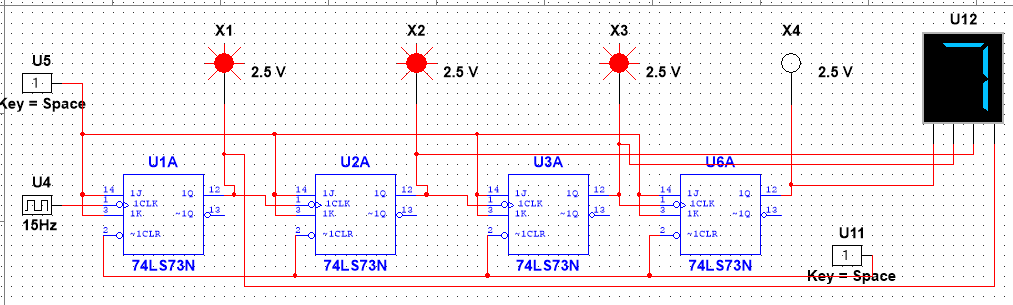
## JK flip flop

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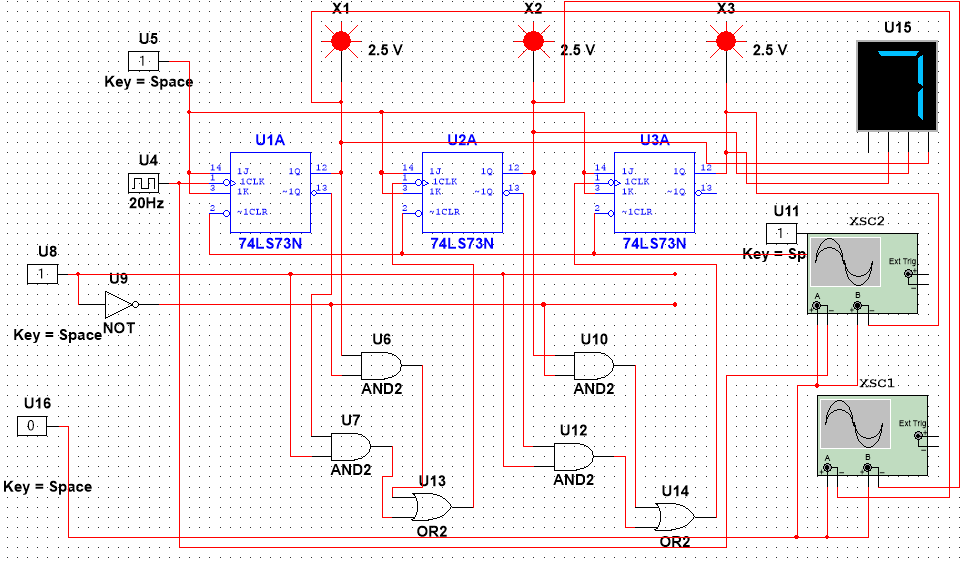
## Asynchronous Decade Counter

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## Asynchronous UP counter

****

## Asynchronous UP DOWN counter

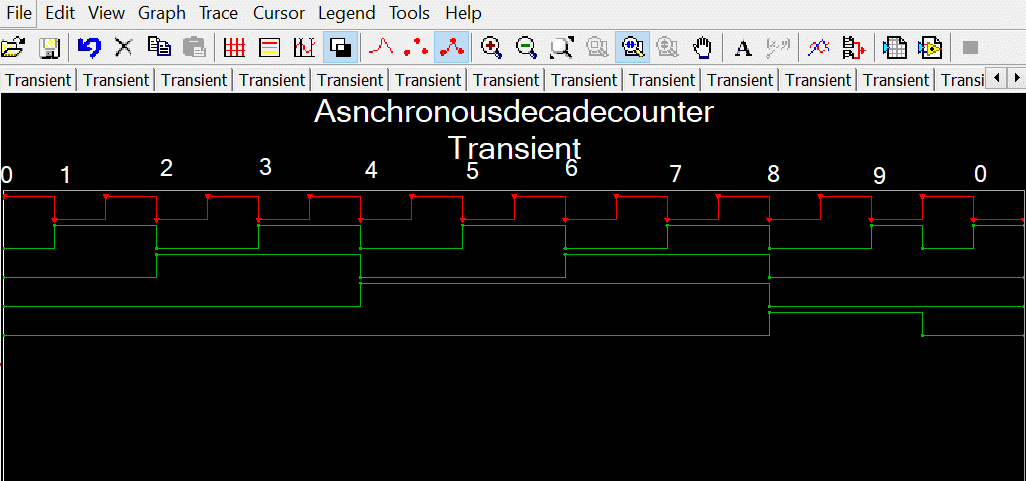
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# Procedure:

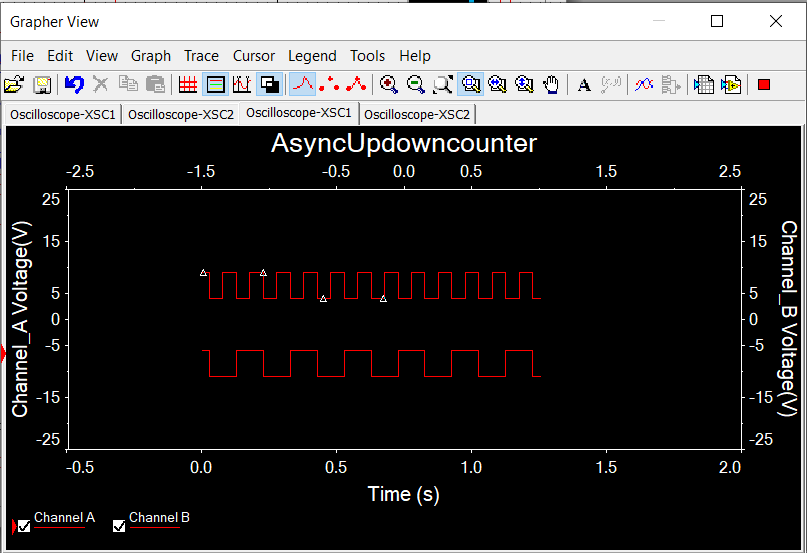
1. Connect the components as shown in the circuit diagram.
2. Give +5V supply to the IC’s.
3. From the LED observe the outputs and also observe the output on 7 Segment LED display.
4. Make a note of the truth tables in the observations.
5. Use DSO / Oscilloscope for observation of various outputs of FFs (timing parameters)
6. Verify the Counting sequence accordingly.

# Observations:

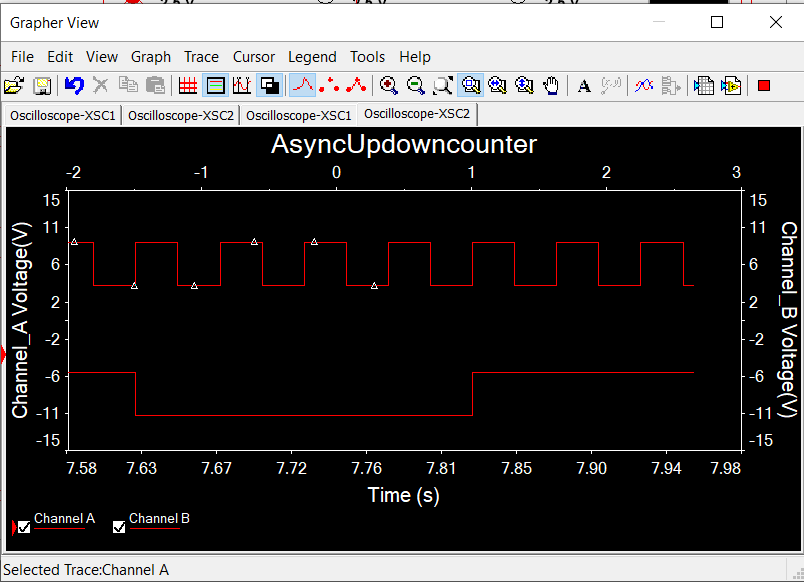
## Asynchronous decade counter



## Shows LSB and Next bit

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## Shows Clock and MSB



# Result:

Above mentioned circuits were created and run in multisim software**.**

# Conclusion:

Truth tables were verified by simulating the created circuit.

# What did you learn?

I learnt how flip flops and asynchronous counters are made, and I understood their working by simulating them and verifying the timing diagrams.Also learnt how to properly use oscilloscope.

**Assignment:**